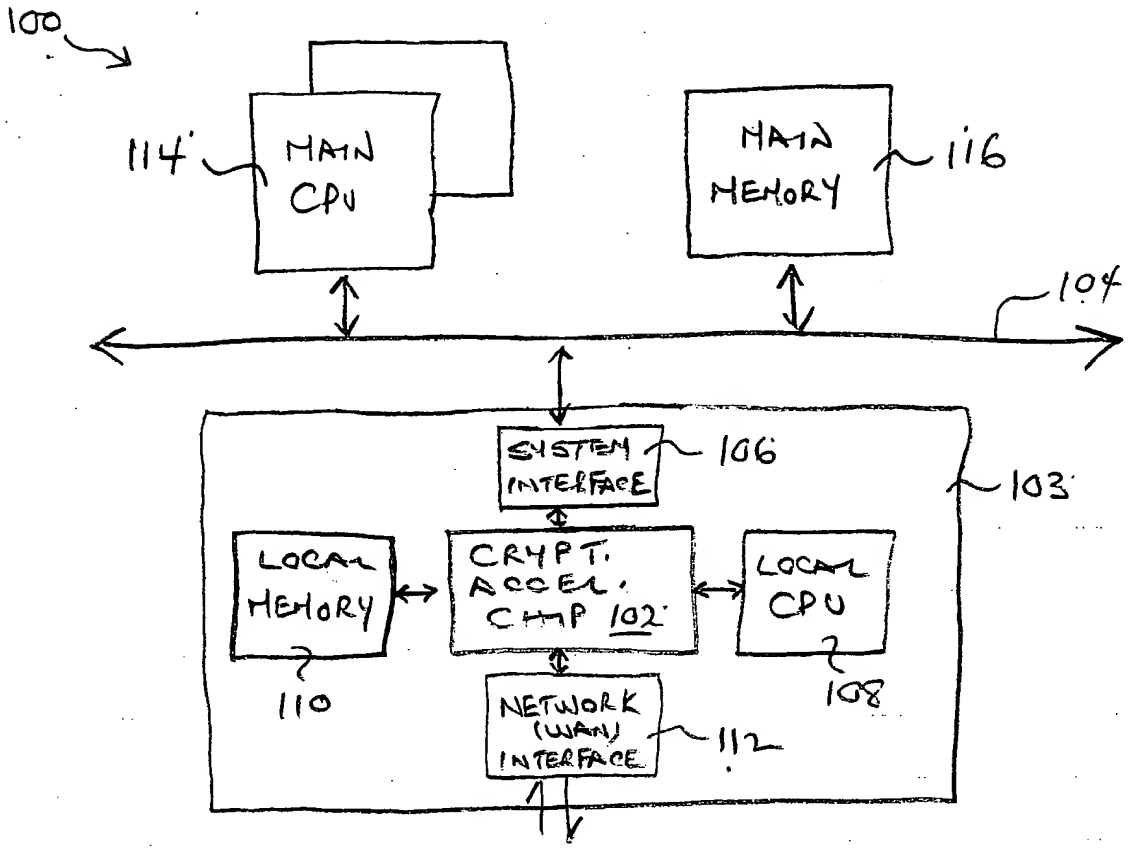
100
114
MAIN CPU
MAIN MEMORY
116
104
SYSTEM INTERFACE
106
103
LOCAL MEMORY
CRYPT. ACCEL. CHIP 102
LOCAL CPU
110
108
NETWORK (WAN) INTERFACE
112

FIG. 1A

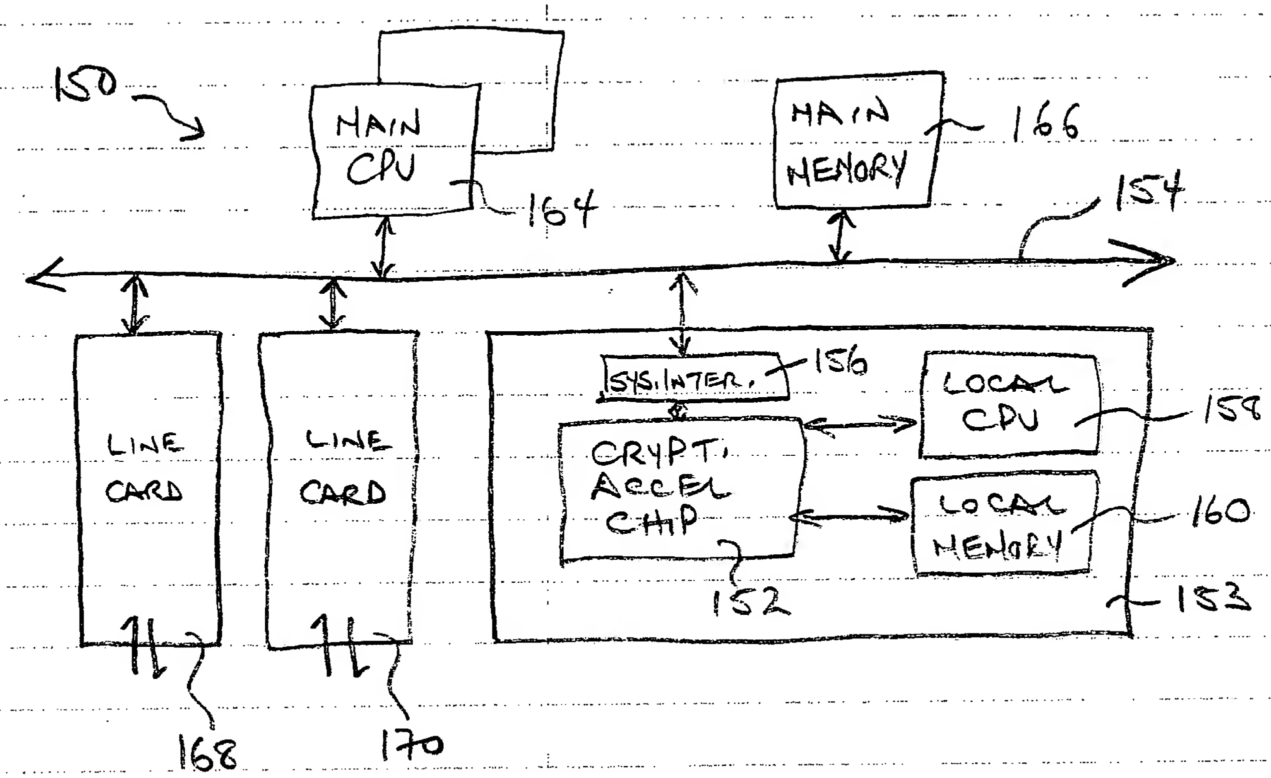
150
MAIN CPU
164
MAIN MEMORY
166
154
LINE CARD
LINE CARD
SYS. INTER.
156
LOCAL CPU
158
CRYPT. ACCEL CHIP
152
LOCAL MEMORY
160
153
168
170

FIG. 1B

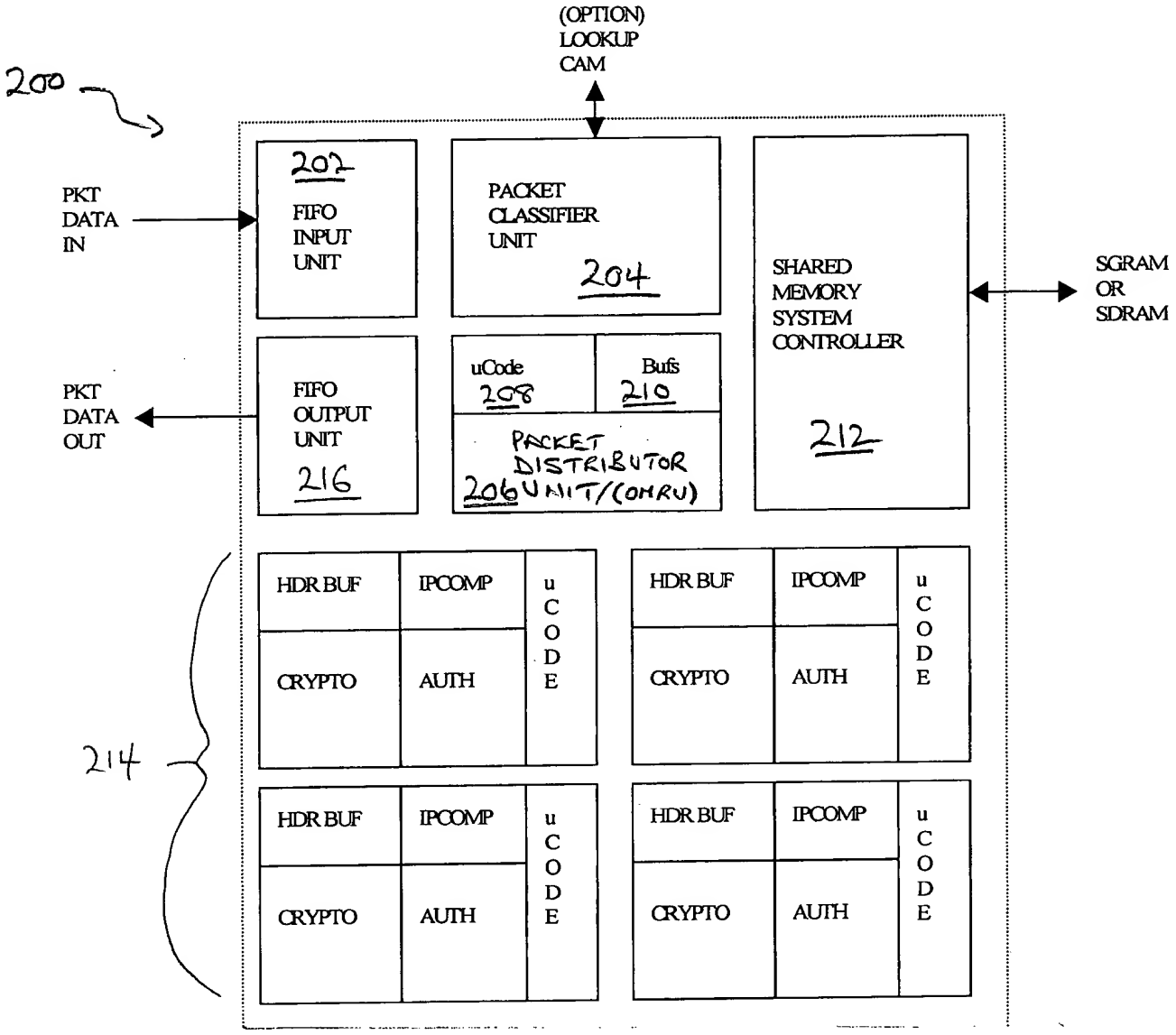
200
(OPTION)
LOOKUP
CAM
202
FIFO
INPUT
UNIT
PKT
DATA
IN
PACKET
CLASSIFIER
UNIT
204
SHARED
MEMORY
SYSTEM
CONTROLLER
212
SGRAM
OR
SDRAM
PKT
DATA
OUT
FIFO
OUTPUT
UNIT
216
uCode
208
Bufs
210
PACKET
DISTRIBUTOR
206 UNIT/(OHRU)
214
HDR BUF
IPCOMP
uCODE
CRYPTO
AUTH

FIG. 2

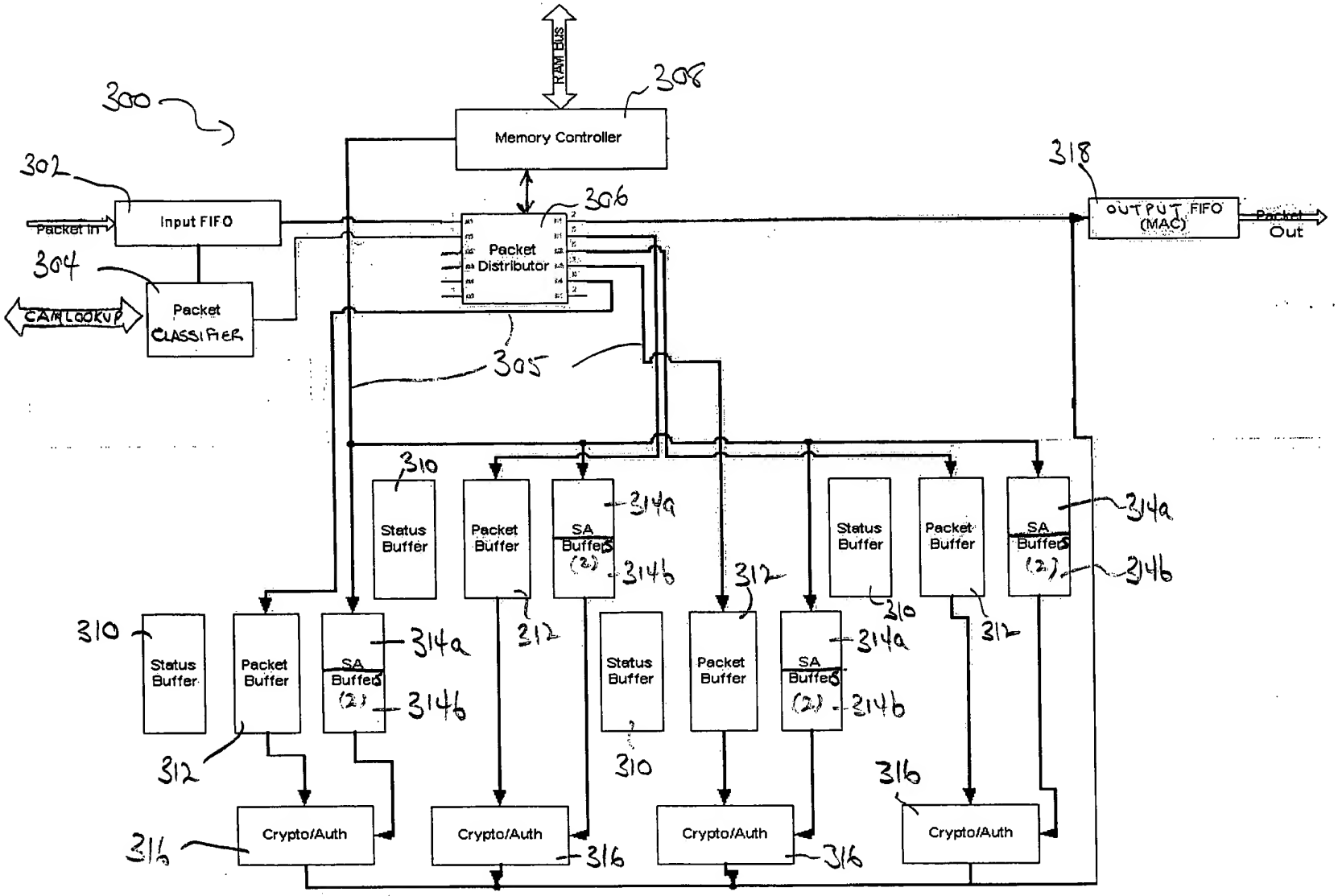

FIG. 3

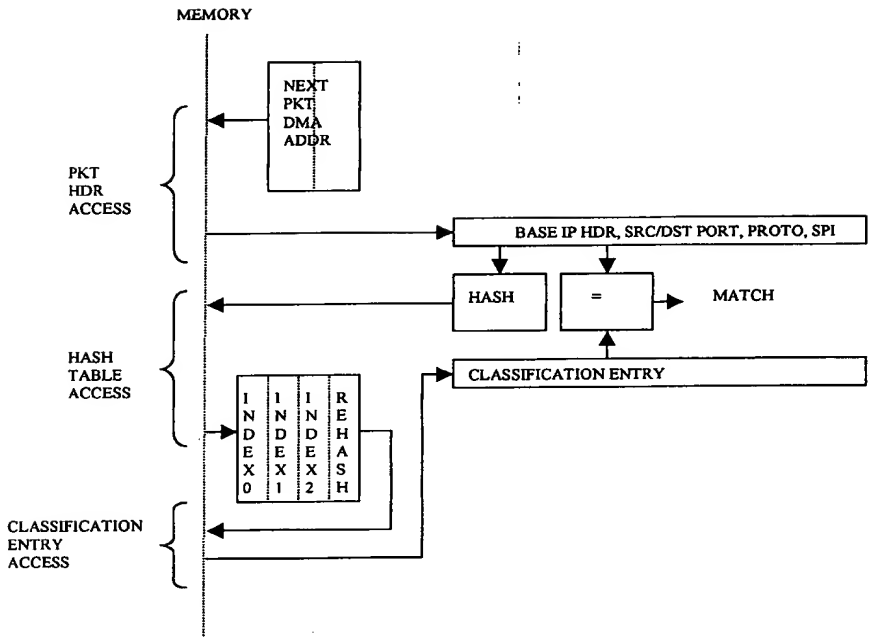
MEMORY
NEXT PKT DMA ADDR
PKT HDR ACCESS
BASE IP HDR, SRC/DST PORT, PROTO, SPI
HASH
=
MATCH
HASH TABLE ACCESS
CLASSIFICATION ENTRY
INDEX0
INDEX1
INDEX2
REHASH
CLASSIFICATION ENTRY ACCESS

FIG. 4

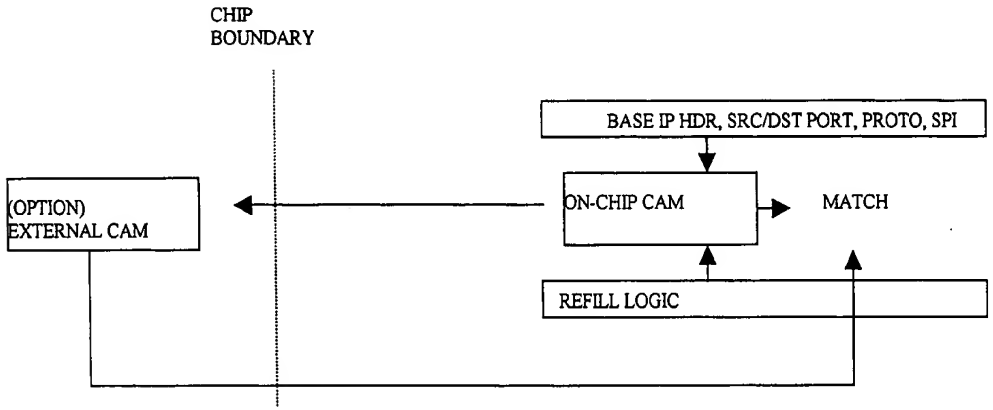
CHIP
BOUNDARY
BASE IP HDR, SRC/DST PORT, PROTO, SPI
(OPTION)
EXTERNAL CAM
ON-CHIP CAM
MATCH
REFILL LOGIC

FIG. 5

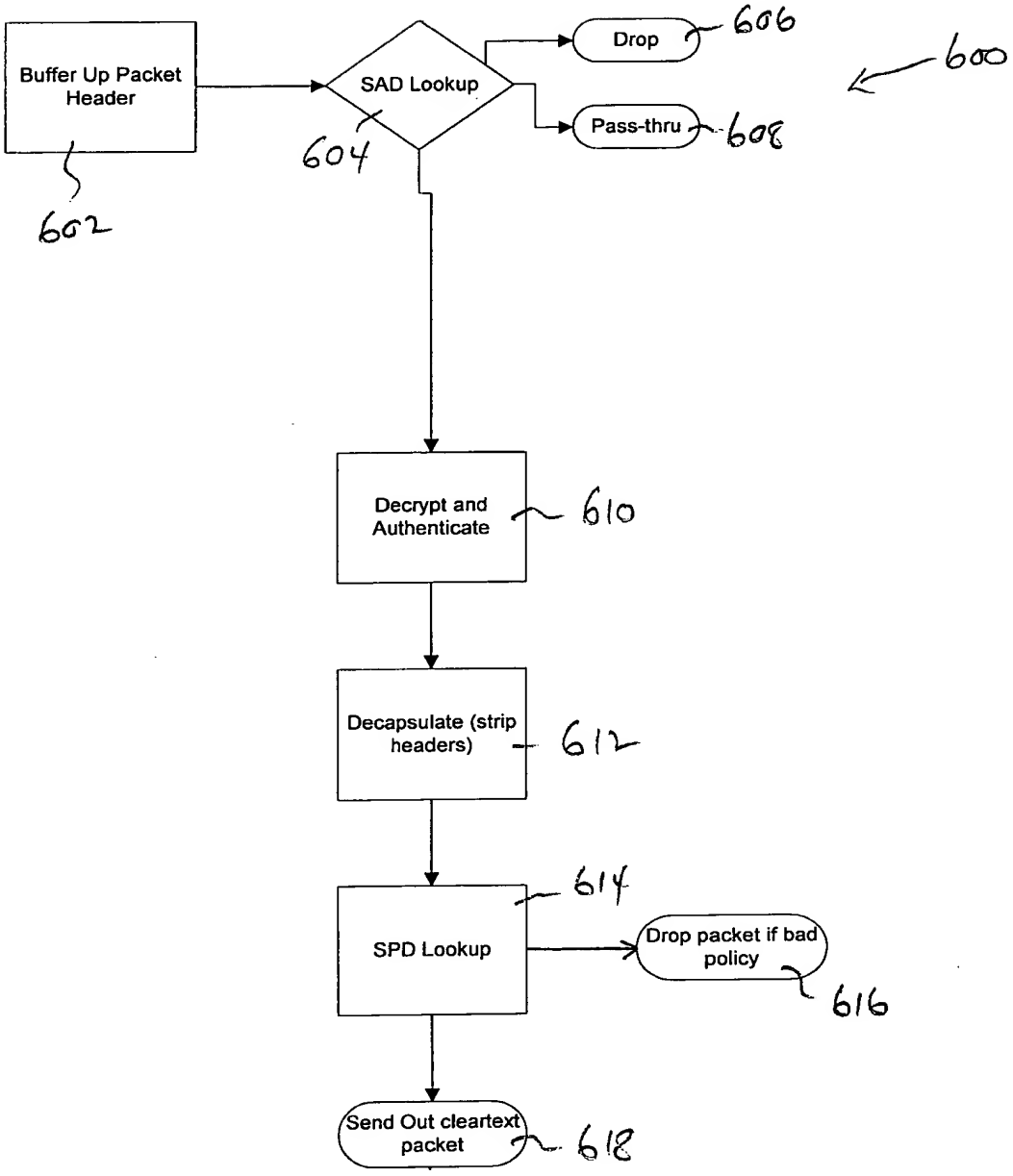
Buffer Up Packet Header
602
SAD Lookup
604
Drop
606
Pass-thru
608
600
Decrypt and Authenticate
610
Decapsulate (strip headers)
612
SPD Lookup
614
Drop packet if bad policy
616
Send Out cleartext packet
618

FIG. 6A

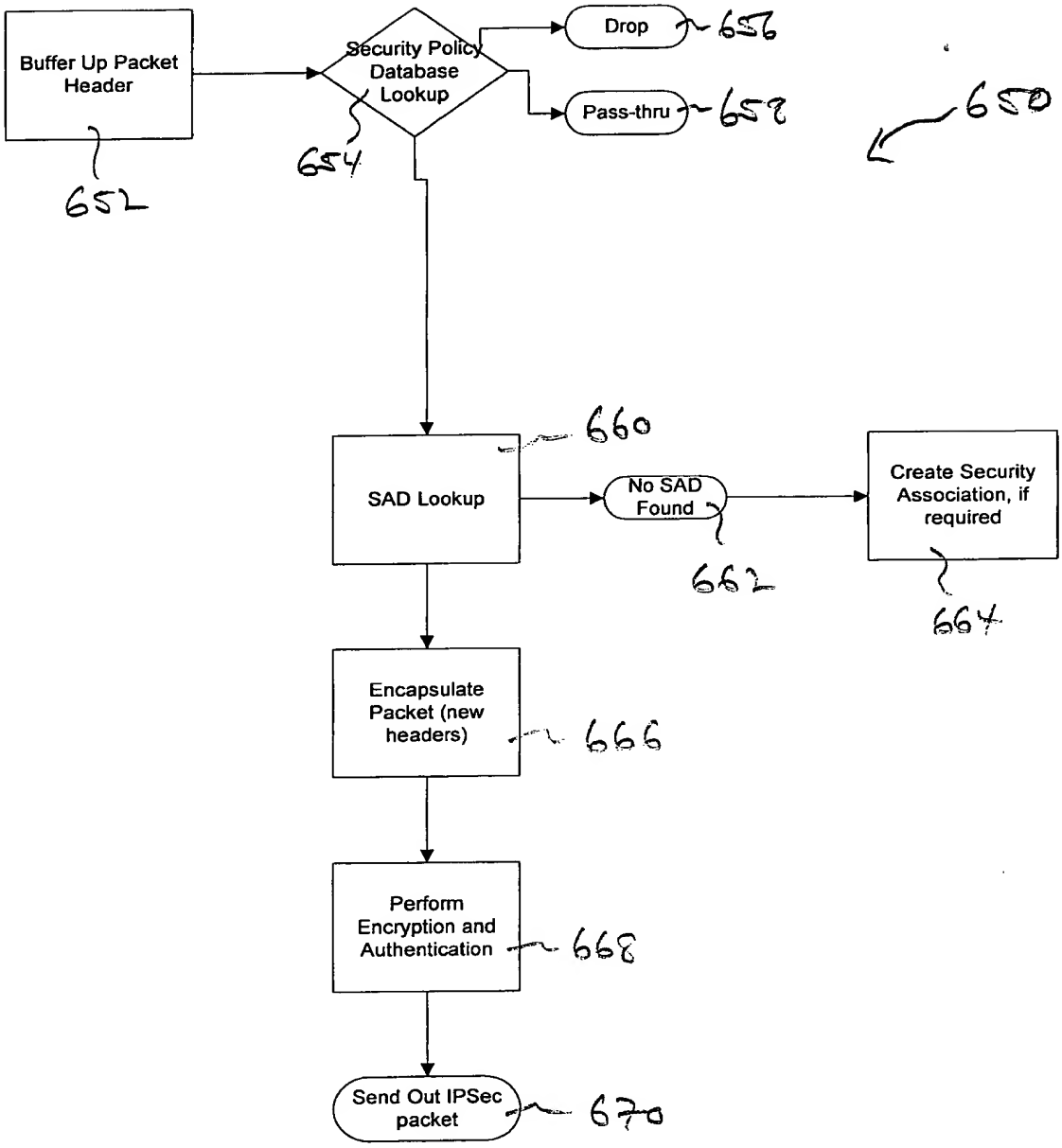
Buffer Up Packet Header
652
Security Policy Database Lookup
654
Drop
656
Pass-thru
658
650
SAD Lookup
660
No SAD Found
662
Create Security Association, if required
664
Encapsulate Packet (new headers)
666
Perform Encryption and Authentication
668
Send Out IPSec packet
670

FIG. 6B

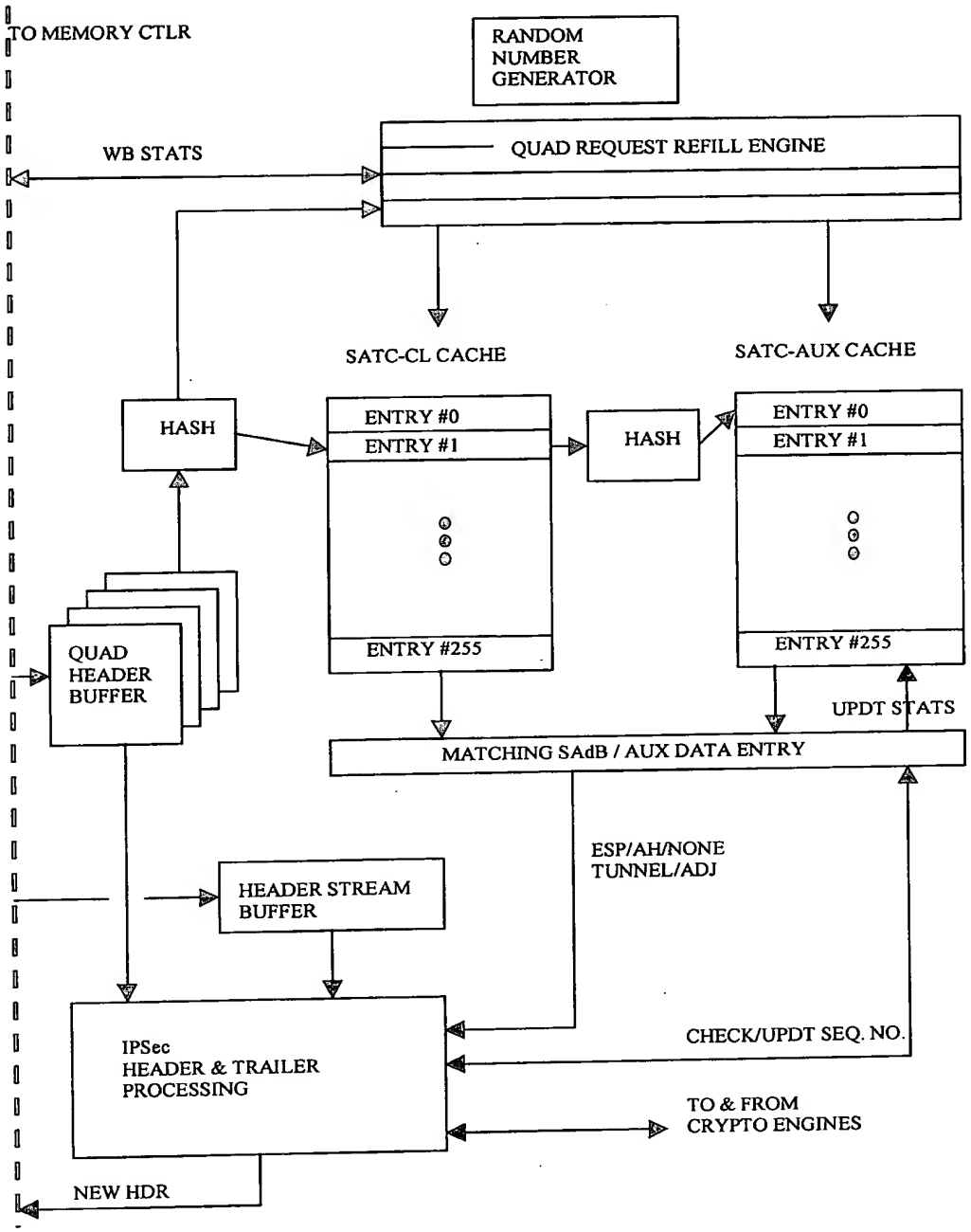
TO MEMORY CTLR
RANDOM NUMBER GENERATOR
WB STATS
QUAD REQUEST REFILL ENGINE
SATC-CL CACHE
SATC-AUX CACHE
HASH
ENTRY #0
ENTRY #1
ENTRY #255
HASH
ENTRY #0
ENTRY #1
ENTRY #255
QUAD HEADER BUFFER
UPDT STATS
MATCHING SAdB / AUX DATA ENTRY
ESP/AH/NONE TUNNEL/ADJ
HEADER STREAM BUFFER
IPSec HEADER & TRAILER PROCESSING
CHECK/UPDT SEQ. NO.
TO & FROM CRYPTO ENGINES
NEW HDR

FIG. 7